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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,114	NGUYEN ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-11,13-18 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-11, 13-18 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 22 and 23 are objected to because of the following informalities:

   a. In claim 22, line 2, please change "move" to "moves", and

   b. In claim 23, line 3, please change "move" to "moves".

2. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6-11, 13-18 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al., US Patent 6,421,774 (hereinafter "Henry"), cited by Examiner on October 5, 2005, in view of Park, US Patent 6,988,190 (hereinafter "Park").

5. Referring to claim 1, Henry has taught for use in a wide-issue processor, a mechanism for conditionally executing instructions, comprising:

   a. a conditional execution block state machine that tags and generates link pointers for instructions located in a conditional execution block (Figure 1, Instruction pointers (IP)/addresses are generated in element 100 for conditional branch instructions to indicate a possible change in flow to a new execution block of instructions., column 6, line 62-column 7, line 44); and

b. conditional link pointer register sets (Figure 1, elements 134, 144, 136, 146, 138, 148, 130, and 140), wherein each of said sets corresponds to a stage of a pipeline of said processor (Figure 1, elements 134 and 144 correspond to the register stage, elements 136 and 146 correspond to the address stage, elements 138 and 148 correspond to the data stage, and elements 130, and 140 correspond to the write back stage.), that contain and cause said link pointers to move through each of said sets as said instructions associated with said link pointers and located in said conditional execution block move through stages (Figure 1, column 7, lines 25-59, elements 134, 144, 136, 146, 138, 148, 130, and 140, Addresses and instructions are piped down through the registers in the various pipeline stages.).

6. Henry has taught pointers that move through the pipeline stages in order to quickly update the branch history table (Figure 1, column 7, lines 25-59). The branch history table is used in predicting conditional branch instructions. Henry has not taught contemporaneous link pointers wherein said link pointers mark at least the beginning and end of a conditional execution block of instructions. However, Park has taught contemporaneous link pointers wherein said link pointers mark at least the beginning and end of a conditional execution block of instructions (Park, column 3, lines 5-27), in order to predict information for conditional repeat execution blocks. Having the pointers of Henry mark the beginning and end of a conditional execution block of instructions, as taught by Park, would have aided in updating the branch history table such that prediction information for conditional repeat execution blocks would have been quickly

updated and predictions would have been provided for conditional repeat execution blocks in addition to branch instruction execution blocks. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the pointers of Henry mark the beginning and end of a conditional execution block of instructions, as taught by Park, for the desirable purpose of updating the branch history table such that prediction information for conditional repeat execution blocks would have been quickly updated and predictions would have been provided not only for branch instruction execution blocks, but also for conditional repeat execution blocks.

7. Referring to claim 2, Henry has taught the mechanism as recited in Claim 1, as described above, and further comprising a conditional execution marking queue, associated with said conditional execution block state machine, that contains ones of said link pointers prior to storage in said sets (Figure 1, Elements 151, 142, and 103 comprise the claimed execution marking queue.).

8. Referring to claim 3, Henry has taught the mechanism as recited in Claim 2, as described above, and wherein said conditional execution marking queue is a five-bit, six-entry queue (Figures 1, 3 and 4, column 10, lines 38-45, At least 12 bits, or entries, are in the queue, so the queue is at least a five-bit, six-entry queue.) and comprises a reordering multiplexer (Figure 1, element 151).

9. Referring to claim 4, Henry has taught the mechanism as recited in Claim 1, as described above, and further comprising a conditional execution attribute register, associated with a group stage of said pipeline, that contains an attribute associated with one of said conditional instructions (column 2, lines 34-61, column 5, line 20-column 6,

line 28, element 103, The branch history bits for instructions are stored in a conditional execution attribute register of the history table in the branch predictor, element 103.).

10. Referring to claim 6, Henry has taught the mechanism as recited in Claim 4, as described above, and further comprising a conditional execution attribute queue that contains attributes read from said conditional execution attribute register (Figure 1, elements 103, 134 136, 138, and 130 comprise the conditional execution attribute queue.).

11. Referring to claim 7, Henry has taught the mechanism as recited in Claim 6, as described above, and wherein said conditional execution attribute queue is of variable depth (column 10, lines 38-44, column 11, lines 21-29, The queue has a depth of N.) and comprises a selecting multiplexer (Figures 1 and 2, element 103, Figure 4, element 414).

12. Claims 8 and 15 do not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

13. Claims 9 and 16 do not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

14. Claims 10 and 17 do not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

15. Claims 11 and 18 do not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

16. Claims 13 and 20 do not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

17. Claims 14 and 21 do not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

18. Referring to claim 22, Henry has taught the mechanism as recited in claim 1, wherein said link pointers move through each register of each register set as at least one instruction move through each of said corresponding stages (column 7, lines 25-45, In Figure 1 of Henry, the pointers move through elements 134, 144, 136, 146, 138, 148, 130, and 140 as the instructions move through each of the Register, Address, Data and Write back stages.).

19. Claim 23 does not recite limitations above the claimed invention set forth in claim 22 and is therefore rejected for the same reasons set forth in the rejection of claim 22 above.

Response to Arguments

20. Applicant's arguments with respect to claims 1-4, 6-11, 13-18 and 20-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

Tonia L. Meonske 10/12/2006

Tonia L. Meonske